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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/715,015
Filing Date: November 17, 2003
Appellant(s): MOON ET AL.

Robert M. Meeks
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 19 June 2006 and 13 September 2007 appealing from the Office action mailed 07 December 2005 (Final Action).

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellants' statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellants' statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,828,612	Yu et al.	10-1998
5,831,924	Nitta et al.	11-1998

Admitted prior art, Figures 1A and 1B, and Specification pp. 1-2.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-7, 9, 10, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art ("Admission") in view of Yu et al. (U.S. Pat. No. 5,828,612).

Admission, in Figs. 1A and 1B, discloses a memory device, and a related method, comprising: a pair of data input/output lines (see for example page 1, line 14 of the instant specification); a delay precharge circuit (1000); a column bank address signal (CBA); a write enable signal (inherent); a precharge circuit (including a PMOS transistor; see page 1, line 12); a precharge control signal (PIOPRB); a first delayed signal (related to the output of 10); a first precharge control signal (related to the output of 15) rising in synchronization with a rising edge of the column bank address signal and falling a first predetermined time period (related to the delay of 10) after an immediately succeeding falling edge of the column bank address signal (see Fig. 1B); precharging after the first predetermined time period following assertion of the column bank address signal when the write enable signal indicates a read operation (see for example

page 2, lines 17-19); a precharge delay control circuit causing application of the first precharge control signal after a read operation (see for example page 2, lines 17-19).

Admission does not disclose a second precharge control signal rising in synchronization with the rising edge of the column bank address signal and falling a second predetermined time period after an immediately succeeding falling edge of the column bank address signal; precharging after the second predetermined time period following assertion of the column bank address signal when the write enable signal indicates a write operation; the precharge delay control circuit causing application of the second precharge control signal after a write operation; selecting one of the first precharge control signal and the second precharge control signal based on a state of the write enable signal; and the first predetermined time period being greater than the second predetermined time period.

However, Yu discloses a first precharge control signal (see /PRECHARGE 110 in Fig. 3 for a READ operation, related to 220 in Figs. 3 and 4) with a first predetermined time period (related to t2 in Fig. 3, corresponding to 206 in Fig. 4); a second precharge control signal (see /PRECHARGE 110 in Fig. 3 for a WRITE operation, related to 218 in Figs. 3 and 4) with a second predetermined time period (related to t5 in Fig. 3, corresponding to 202 in Fig. 4); the second predetermined time period being shorter than the first predetermined time period (i.e., t5 is shorted than t2; see Fig. 3); a write enable signal (R/W 102); and selecting (via a selection means that includes 306, 302 and 210 in Fig. 4) the first precharge control signal for a read operation and the second precharge control signal for a write operation, based on the state of the write enable signal (see /PRECHARGE 110 in Fig. 3).

In view of Yu's teaching of the advantages of having different and independently optimized precharge delay depending on the type of access operation (see for example Yu, column 2, lines 36-41), it would have been obvious at the time the invention was made to a person having ordinary skill in the art, who is familiar with Admission, to modify the device and the related method of Admission to generate a second precharge control signal responsive to the bank address signal (in a manner similar to that of Yu, or Fig. 1A of Admission, but with a shorter delay than that of the first precharge control signal, as in Yu), and to select the first precharge control signal for a read operation and the second precharge control signal for a write operation, determined by the write enable signal (for example, using a selection means similar to that of Yu, or a multiplexer commonly used and well known in the art), for the purpose of increasing the frequency of operation (see, for example, Yu, column 2, lines 36-41).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art ("Admission") in view of Yu et al. (U.S. Pat. No. 5,828,612) as applied to claim 6 above, and further in view of Nitta et al. (U.S. Pat. No. 5,831,924).

The above Admission/Yu combination discloses a memory device as recited in claim 6, with the exception of the pair of data input/output lines being a pair of global input/output lines. Nitta discloses a pair of global input/output lines that are precharged (see for example column 3, lines 37-42). Since memories having a pair of global input/output lines that are precharged were common and well known in the art (as exemplified by Nitta), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the precharging

means of the Admission/Yu combination to such memories, for the purpose of increasing the frequency of operation in such memories (see for example Yu, column 2, lines 36-41).

(10) Response to Argument

First, Appellants' references to various MPEP sections and case laws, on page 4 of the Brief, are acknowledged; however, as will be noted below, the outstanding ground(s) of rejections presented in the Final Action meet the requirements of the cited MPEP sections and case laws.

Regarding independent claim 1, in the first paragraph on page 5 of the Brief, Appellants state that "[r]ather, FIGs. 1A and 1B describe a circuit that generates a precharge control signal responsive only to a column bank address signal CBA."

It is noted that, in addition to generating a precharge control signal responsive to a column bank address signal CBA, FIGs. 1A and 1B of Admission also discloses generating a delayed signal (or a first delayed signal of claim 1, related to the output of 10) from the column bank address signal (CBA) that is delayed by a time period (or a first time period of claim 1, related to the delay of 10) with respect to the column bank address signal (CBA), and a precharge control signal (or a first precharge control signal of claim 1, related to the output of 15) generated from the delayed signal (or the first delayed signal of claim 1).

Appellants argue, in the bottom paragraph on page 5 of the Brief, that "[i]n particular, Yu does not generate 'first and second delayed signals from the column address bank signal that are

delayed by respective different first and second time periods with respect to the column bank address signal' and does not apply 'to the precharge circuit, responsive to a precharge delay control signal, a selected one of a first precharge control signal generated from the first delayed signal and a second precharge control signal generated from the second delayed signal.'"

In response, it is noted that, although Yu does not disclose a column bank address signal, Yu does disclose generating first and second delayed signals (the output of 206 and 202, respectively, in Fig. 4, corresponding to DEFAULT PRECHARGE TRIGGER 216 and WRITE PRECHARGE TRIGGER 212, respectively, in Figs. 3 and 4) from a clock signal (CLK 104 in Figs. 3 and 4) that are delayed by respective different first and second time periods (t2 of DEFAULT PRECHARGE TRIGGER 216 in Fig. 3, and t5 of WRITE PRECHARGE TRIGGER 212 from a falling edge of CLK 104 in Fig. 3, the time periods associated with 206 and 202, respectively, in Fig. 4) with respect to the clock signal, and applying to a precharge circuit (via 110 in Fig. 4), responsive to a precharge delay control signal (WRITE PRECHARGE ENABLE 210 in Figs. 3 and 4), a selected one (selected via 306, in conjunction with 302 and WRITE PRECHARGE ENABLE 210 in Figs. 3 and 4) of first precharge control signal (/READ PRECHARGE 220 in Figs. 3 and 4) generated from the first delayed signal (DEFAULT PRECHARGE TRIGGER 216 in Figs. 3 and 4) and second precharge control signal (/WRITE PRECHARGE 218 in Figs. 3 and 4) generated from the second delayed signal (WRITE PRECHARGE TRIGGER 212). Further, it is Admission, in combination with Yu, that discloses the column bank address signal from which the first and second delayed signals would be generated.

Appellants further argue, in the bottom paragraph on page 5 of the Brief, that "[r]ather, Yu generates only a DEFAULT PRECHARGE TRIGGER (see Yu, FIGs. 2 and 4) responsive to an address signal Ax."

In response, it is noted that DEFAULT PRECHARGE TRIGGER 216 of Yu in Figs. 2-4 is not the only signal generated in Yu. In addition, more importantly for the timing purposes, DEFAULT PRECHARGE TRIGGER 216 is responsive also to a clock signal CLK 104 (see Figs. 3 and 4 of Yu), and is related to /READ PRECHARGE 220 in Figs. 3 and 4, which is a precharge control signal for a read operation.

Appellants further argue, in the bottom paragraph on page 5 of the Brief, that "there is nothing in Yu corresponding to the recited 'first and second delayed signals' or the recited 'first precharge control signal generated from the first delayed signal and a second precharge control signal generated from the second delayed signal.' Accordingly, even if combined, Admission and Yu do not disclose or suggest all of the recitations of independent Claim 1."

In response, as noted earlier, it is noted that Yu does disclose first and second delayed signals (the output of 206 and 202, respectively, in Fig. 4, corresponding to DEFAULT PRECHARGE TRIGGER 216 and WRITE PRECHARGE TRIGGER 212, respectively, in Figs. 3 and 4), and first precharge control signal (/READ PRECHARGE 220 in Figs. 3 and 4) generated from the first delayed signal (DEFAULT PRECHARGE TRIGGER 216 in Figs. 3 and 4) and a second precharge control signal (/WRITE PRECHARGE 218 in Figs. 3 and 4) generated from the second delayed signal (WRITE PRECHARGE TRIGGER 212), as recited in

claim 1; therefore, the combination of Admission and Yu discloses all of the recitations of independent Claim 1.

Appellants further argue, in the first and second paragraphs on page 6 of the Brief, that "the Final Action provides insufficient evidence of a motivation or suggestion to combine Admission and Yu. As noted above, Yu describes a technique for providing different precharge timings for read and write cycles, but this is not clear and particular evidence of a teaching or suggestion to modify the device described in the Background of the Invention in the specific manner recited in Claim 1, as neither Yu nor the Background of the Invention disclose or suggest this specific approach," and that "[t]he reasoning provided on pages 4 and 7 of the Final Action as a basis for modifying the device described in the Background is erroneous," and quotes from page 4 of the Final Action. Appellants further argue that "[t]his reasoning relies on a series of inferences that are not supported by the prior art in evidence. In particular, as noted above, Yu already proposes a different way of generating different read and write cycle precharge timings, one that does not involve the operations described in the above-quoted passage from page 4 of the Final Action. The Final Action provides no evidence from the prior art as to how or why applying this approach to the circuitry described in the Background of the Invention would result in the recitations of Claim 1."

In response, it is noted that Appellants have incompletely quoted Examiner's statement of motivation to combine Admission and Yu, from page 4 of the Final Action. Specifically, in the Final Action, Examiner has clearly cited an evidence from the Yu reference itself to combine Admission and Yu, namely, column 2, lines 36-41 of Yu (see also page 4 of the Final Action).

Further, as noted earlier, the combination of Admission (the device described in the Background of the Invention) and Yu does disclose a device as recited in Claim 1.

Appellants further argue, in the second paragraph on page 6, that "[m]oreover, references to addition of a 'multiplexer' and other modifications of the circuitry described in the Background of the Invention are simply hindsight reconstruction, unsupported by any particular evidence from the prior art. Accordingly, Appellants submit that the Final Action fails to provide the requisite evidence of a suggestion or motivation to combine Admission and Yu in the manner proposed in the Final Action."

In response, as noted earlier, it is noted that the Yu reference itself does disclose a selection means (including 306, 302 and 210 in Figs. 3 and 4) for selecting between the first and second precharge control signals, and does provide an evidence of a motivation to combine Admission and Yu in the manner proposed in the Final Action (see Yu, column 2, lines 36-41). Further, it is noted that a "multiplexer" was cited as an example of another alternative signal selection means commonly used and well known in the art. It is also noted that a "multiplexer" per se is not described in the Background of the Invention.

Appellants present, starting at the bottom of page 6 of the Brief, similar arguments for independent claims 6, 9 and 15.

In response, since no new arguments specific to these claims have been presented, the above response with respect to claim 1 is noted herein.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Primary Patent Examiner, Art Unit 2824
04 October 2007

Conferees:

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10/4/07